In the Specification

Amend the following numbered paragraphs of the specification:

[0027] Read operation is shown in Figure 3 by an initialization signal that is applied at 126 (FCLRN) which pulses low to initialize (L1) 103 latch input (FT) 122 to a high state. A current level is set from current source 116 by reference level (VSWITCH) 106 and this predetermined amount of current I0 flows into efuse 101 when (FSETP) 114 activates set device 120 and shunt device 131. The voltage at (L1) 103 input node (FT) 122 is now essentially a function of the current (I0 * R_efuse). The resistive effects of all other devices conducting I0 are compensated out by Reference Generator 200 in Fig. 5 and will be discussed hereinafter. If the fuse resistance R_efuse is BELOW the desired latch trip point or unity gain point, the voltage on input node (FT) ~~112~~ 122 will be BELOW the latch-voltage trip point and the latch will change from its first initialized state to a second low state. If R_efuse has a resistance HIGHER than the desired latch trip point then the voltage on input node (FT) 122 will be HIGHER than the latch-voltage trip point and the latch will remain in its initialized first state.

[0028] Another feature of this circuit is to provide an isolation buffer 102 in the latch feedback path to maintain the gate of feedback devices 125 at ground to achieve constant conduction during sensing. This is essential for accurate calculation of the resistive trip point of the latch by the Reference Current Generator circuit 200 shown in Fig. 5. Local decoupling on the (VSWITCH) 106 reference line is provided by capacitor 124.

[0029] The present invention uses an active circuit with feedback to find a reference current which will make the latch input voltage equal to the latch-inverter trip point at a selectable fuse resistance value. Referring to Figure 5, a latch-mimic circuit receives this reference current and the latch-input voltage is monitored by the (+) input of a diff-amp, which is compared to the latch-inverter trip point(-) as calculated by the reference inverter (I5R) biased at its trip point. The diff-amp outputs a voltage (VSWITCH) which will bias the current source in the latch-mimic circuit such that the (-) and (+) terminals are substantially equal to zero. This makes the latch input voltage equal to the latch-inverter switch point at the selected fuse resistance.In order for the current reference generator to work well, the L1 latch in 103 must switch as an ~~interter~~ inverter - not as a latch. This means the feedback devices coupled to the latch input nodes 125, 127 must be completely on or off during switching so as not to add some unpredictable current into the input node during switching. In a simple latch design, as the output switches the output creeps up a fraction of a volt. This fraction of a volt when coupled to the feedback devices alters their conduction and further enhances switching by altering the switch point until the latch flips. A latch switch point is dynamic, it changes during switching. It is necessary to stabilize the latch trip point to make it predictable and equate it to the latch input voltage. The latch trip point is held constant by preventing creep-up of the feedback gates by inclusion of the 2 feedback isolation inverters (102). They act as a filter or buffer and will not propagate a partial level, but switch when the input inverter 128 is fully switched.

[0031] A further feature of the present invention is to provide a variable trip point latch with the ability to sense a fuse using a first reference current level and once sensing mode is completed, maximize this current to provide larger latch-feedback current to enhance soft error upset Soft Error Upset (SEU) immunity. This is done by allowing the (VSWITCH) 106 level to be controlled by Reference Current ~~Level~~ Generator 200 during sensing and margin testing, but disabling it and clamping it to GND for normal operation. With (VSWITCH) 106 at GND, current control device 116 provides its maximum current into L1 latch 103. In an SEU node (FT) 122 is partially discharged toward GND, and with current supply device 116 providing its maximum level it is now able to supply typically 10X more current than it could when at its appropriate level for a trip point of 100K-ohms. Hence, the first current level is optimized for fuse reading and is only utilized at power up which reduces the window of vulnerability to a fraction of a second. The second full-on state is present for the thousands of power-on hours over the life of the circuit.

[0032] The (VSWITCH) 106 current reference is created by Reference Current Generator ~~20~~ 200 in Fig. 5. It consists of a Resistor selection block 201, an inverter switch point reference 202, operational amplifier 203, latch mimic 204 and disable phase generator 205. The object of circuit 200 is to provide a reference level on output VSWITCH which will provide appropriate current into variable trip point latch circuit(s) 100 in order to accurately preselect its resistive trip point. A further object of this circuit is to provide compensation means so as to make any trip point variations from process, voltage and temperature (PVT) essentially zero. In operation, if a resistive trip point of 100K-ohms is desired for example, the Resistor selection block 201 is set to a resistor value of 100K-ohms by appropriate selection of digital control word RES_SEL (0-n) 206 to select the correct series resistance in this digital to resistance converter. Inverter switch point reference 202 will output the unity gain point of the inverter I5R having beta ratios and geometry identical to its corresponding inverter 128 in the variable trip point latch 100 in Figure 1. Decap capacitor C1 offsets displacement noise from op-amp 203. VREF provides a target for node VLAT to follow. Latch mimic 204 represents all the series impedances present in the I0 current path in latch 100. Op amp 203 uses negative feedback to find a voltage VSWITCH which will make node VLAT essentially equal to the latch inverter 128 switch point when the "fuse" resistance is 100K-ohms. Once generated by this low current circuit, VSWITCH is applied to multiple fuse latch 100 circuits to control the resistive trip point of all in unison. Large decap capacitor C0 is used to offset displacement current from latch circuits 100 and line to line noise.

[0034] ~~This circuit~~ Reference Current Generator 200 will adjust the VSWITCH point to gate the proper amount of current into the fuse latch current device 116 to insure the latch inverter 128 will switch when the fuse resistance is at a predetermined value. If the switch point of 128 changes due to PVT, then (VSWITCH) 106 level changes accordingly. As other element values change from PVT, the VSWITCH level will adjust to keep the resistive trip point constant. Larger than minimum geometry devices are used in the circuit layout to improve parametric tracking between the ~~reference circuit~~ Reference Current Generator 200 and the fuse latches 100.

[0036] It is envisioned that other designs may be used for construction of a compensated variable resistance fuse latch similar to those discussed above. For example, the latch could use an NFET current mirror instead of a PFET with similar and appropriate changes to Reference Current Generator ~~Circuit~~ 200. The SEU enhancement could come from an additional current supply

device in parallel with current source 116 which is switched on after fuse read. It should be understood that the variable trip point latch does not need to be an (L1)(L2) scanable latch, and could be a simpler latch employing a simple cross-coupled latch for 103, however accuracy may be traded for simplicity in many of these alternate embodiments.